

**REMARKS**

Claims 1-8, 11-15, 20-24, 26 and 30 are pending in this application. By this Amendment, 1, 5, 7, 11, 13, 22-24, and 26 are amended. Support for the amendment to claims 1, 5, 7, 11, 13, 22-24 and 26 can be found, for example, in the specification at page 11, paragraphs [0079] to [0081]. No new matter is added.

The courtesies extended to Applicants' representative by Examiner Boddie at the interview held April 19, 2007, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicants' record of the interview.

Claims 1-8, 11, 12, 20-24 and 30 were rejected under 35 U.S.C. §103(a) over Ohtaka et al. (U.S. Patent No. 6,151,000) in view of Asano (U.S. Patent No. 6,975,290); and claims 13-15 and 26 were rejected under 35 U.S.C. §103(a) over Ohtaka and Asano and further in view of Wakitani et al. (U.S. Patent No. 5,940,142). The rejections are respectfully traversed.

As agreed in the personal interview, the applied prior art does not teach the reset transistor and associated features recited in the independent claims.

Applicants respectfully request the rejections be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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